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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,906	11/26/2003	Wolfgang Hetzel	MAS-FIN-419	1149

24131 7590 10/20/2004

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,906	HETZEL ET AL.	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Group I, Claims 1-9, in the reply filed on 08/30/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group I, Claims 1-9 in the reply filed on 08/30/04 is acknowledged.

Claims 10-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/30/04.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho (PN 6,087,718, of record).

Cho discloses, as shown in Figure 2, an electronic component, comprising:

a chip stack including a first semiconductor chip (5) and a second semiconductor chip (7);

a plurality of flat conductors (2), each one of the plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section, the inner section of each one of the plurality of flat conductors and the central section of each one of the plurality of flat conductors configured between the first semiconductor chip and the second semiconductor chip;

a package;

a plurality of first bonding connections (9);

a plurality of second bonding connections (9);

the first semiconductor chip having a plurality of bonding surfaces;

the second semiconductor chip having a plurality of bonding surfaces;

each one of the plurality of first bonding connections connecting one of the plurality of bonding surfaces on the first semiconductor chip to the inner section of one of the plurality of flat conductors;

each one of the plurality of second bonding connections connecting one of the plurality of bonding surfaces on the second semiconductor chip to the transitional section of one of the plurality of flat conductors.

With regard to claim 2, Cho discloses one of the plurality of first bonding connections is connected to the inner section of a given one of the plurality of flat conductors; and

one of the plurality of second bonding connections is connected to the transitional section of the given one of the plurality of flat conductors.

With regard to claim 3, Cho discloses the plurality of bonding surfaces on the first semiconductor chip and the plurality of bonding surfaces on the second semiconductor chip are configured at mutually congruent positions.

With regard to claim 4, Cho discloses the first semiconductor chip includes a bonding channel and the second semiconductor chip includes a bonding channel congruently configured with respect to the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the first semiconductor chip are configured in the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the second semiconductor chip are configured in the bonding channel of the second semiconductor chip

With regard to claim 6, Cho discloses the first semiconductor chip includes an active upper face mounted on the central section of each one of the plurality of flat conductors; and

the second semiconductor chip includes a rear face mounted on the central section of each one of the plurality of flat conductors.

With regard to claim 8, Cho discloses the first semiconductor chip includes an active upper face;

the second semiconductor chip includes an active upper face;

the outer section of each one of the plurality of flat conductor has a z-shaped bend aligned such that the active upper face of the first semiconductor chip and the active upper face of the second semiconductor chip are aligned in a direction opposite the bends.

3. Claims 1-4 and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (PN 6,483,181).

Chang et al. discloses, as shown in Figures 2 and 4, an electronic component, comprising:

a chip stack including a first semiconductor chip (210) and a second semiconductor chip (220);

a plurality of flat conductors (230), each one of the plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section, the inner section of each one of the plurality of flat conductors and the central section of each one of the plurality of flat conductors configured between the first semiconductor chip and the second semiconductor chip;

a package;

a plurality of first bonding connections (270);

a plurality of second bonding connections (270);

the first semiconductor chip having a plurality of bonding surfaces;

the second semiconductor chip having a plurality of bonding surfaces;

each one of the plurality of first bonding connections connecting one of the plurality of bonding surfaces on the firs semiconductor chip to the inner section of one of the plurality of flat conductors;

each one of the plurality of second bonding connections connecting one of the plurality of bonding surfaces on the second semiconductor chip to the transitional section of one of the plurality of flat conductors.

With regard to claim 2, Chang et al. discloses one of the plurality of first bonding connections is connected to the inner section of a given one of the plurality of flat conductors; and

one of the plurality of second bonding connections is connected to the transitional section of the given one of the plurality of flat conductors.

With regard to claim 3, Chang et al. discloses the plurality of bonding surfaces on the fist semiconductor chip and the plurality of bonding surfaces on the second semiconductor chip are configured at mutually congruent positions.

With regard to claim 4, Chang et al. discloses the first semiconductor chip includes a bonding channel and the second semiconductor chip includes a bonding channel congruently configured with respect to the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the first semiconductor chip are configured in the bonding channel of the first semiconductor chip;

the plurality of bonding surfaces on the second semiconductor chip are configured in the bonding channel of the second semiconductor chip

With regard to claim 6, Chang et al. discloses the first semiconductor chip includes an active upper face mounted on the central section of each one of the plurality of flat conductors; and

the second semiconductor chip includes a rear face mounted on the central section of each one of the plurality of flat conductors.

With regard to claim 7, Chang et al. discloses the first semiconductor chip includes an active upper face;

the second semiconductor chip includes an active upper face;

the outer section of each one of the plurality of flat conductor has a z-shaped bend aligned such that the active upper face of the first semiconductor chip and the active upper face of the second semiconductor chip are aligned in a direction of the bends.

With regard to claim 8, Chang et al. discloses the first semiconductor chip includes an active upper face;

the second semiconductor chip includes an active upper face;

the outer section of each one of the plurality of flat conductor has a z-shaped bend aligned such that the active upper face of the first semiconductor chip and the active upper face of the second semiconductor chip are aligned in a direction opposite the bends.

With regard to claim 9, Chang et al. discloses the second semiconductor chip includes an active an upper face; and

the transitional section of each one of the plurality of flat conductors has a bend toward the active upper face of the second semiconductor chip.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (PN 6,087,718, of record) in view of Chang et al. (PN 6,483,181).

Cho discloses the claimed invention including the electronic component as recited in the rejection above. Cho does not disclose the active upper face of the first semiconductor chip and the active upper face of the second semiconductor chip are aligned in direction of the bend or bond toward the active upper face of the second semiconductor chip. However, Chang et al. discloses the active upper face of the first semiconductor chip and the active upper face of the second semiconductor chip are aligned in direction of the bend or opposite the bend or bond toward the active upper face of the second semiconductor chip. Note Figures 2 and 4 of Chang et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to align the first chip and the second chip of Cho in direction of bend, such as taught by Chang et al. depend on the desired configuration of the design.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (PN 6,087,718, of record) in view of Reference K (DE 100 03 670, of record).

Cho discloses the claimed invention including the electronic component as recited in the rejection above. Cho does not disclose the component further comprising an interposer layer between the upper surface of the chips and the plurality of bonding surfaces. However, Reference discloses a component further comprising an interposer layer between the upper surface of the chips and the plurality of bonding surfaces. Note Figures 3 and 6. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an interposer layer between the upper surface of the chips and the plurality of bonding surfaces of Cho, such as taught by Reference K, in order to protect and prevent the upper surface of the chip from cracking and damage.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (PN 6,483,181) in view of Reference K (DE 100 03 670, of record).

Chang et al. discloses the claimed invention including the electronic component as recited in the rejection above. Chang et al. does not disclose the component further comprising an interposer layer between the upper surface of the chips and the plurality of bonding surfaces. However, Reference discloses a component further comprising an interposer layer between the upper surface of the chips and the plurality of bonding surfaces. Note Figures 3 and 6. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an interposer layer between the upper surface of the chips and the plurality of bonding

surfaces of Chang et al., such as taught by Reference K, in order to protect and prevent the upper surface of the chip from cracking and damage.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

September 28, 2004

Hung Vu

Patent Examiner